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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/621,504 | 07/17/2003 | Martin Mallinson | 37213.01000 | 2600 |

7590 01/13/2005

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| **ART UNIT** | **PAPER NUMBER** |
| 2644 | |

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/621,504 | MALLINSON, MARTIN | |
| | Examiner | Art Unit | |
| | Andrew C Flanders | 2644 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-73* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-73* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9 Sept 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claim 17 is objected to because of the following informalities: Claim 17 should apparently depend on claim 15. For the purpose of expediting prosecution, claim 17 will be understood to depend on claim 15 for this office action. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 11, 12, 21, 23-26, 28, 29, 31, 34, 42, 47 – 54, 56, 57, 61 – 64, 68 and 73 are rejected under 35 U.S.C. 102(b) as being anticipated by Ruha (U.S. Patent 6,466,087).

4. Regarding Claims 1, 23, and 24, Ruha discloses a pulse width modulator (fig. 4 element 12) a clock which affects the resolution of the PWM (col. 6 lines 49 – 50) (i.e. a pulse width modulator having a clock rate) and an error measurement block that includes a digital filter (fig. 4 elements 16 and fig. 6B element 16c) which receives an input from the pulse width modulator (fig 4 element 14) and the circuitry operates to minimize noise in the signal applied to the load (col. 6 lines 62 – 63) (i.e. a digital filter configured to receive an output of said pulse width modulator, wherein said output comprises a distortion, and wherein said digital filter samples said output at said clock rate to suppress said distortion).

5. Regarding Claims 2 and 25, in addition to the elements stated above regarding claims 1 and 24, Ruha discloses a sigma delta modulator that interpolates an input signal to an over sampled lower resolution (col. 4 lines 23 – 25) (i.e. an over sampling modulator).

6. Regarding Claims 3 and 26, in addition to the elements stated above regarding claims 2 and 25, Ruha discloses a signal delta modulator (col. 4 lines 23 – 35).

7. Regarding Claims 4 and 28, in addition to the elements stated above regarding claims 3 and 25 , Ruha shows a sigma delta modulator upstream of a pulse width modulator (fig. 4 elements 11 and 12).

8. Regarding Claims 5 and 29, in addition to the elements stated above regarding claims 4 and 28, Ruha discloses the output from the sigma-delta modulator has $2^n$ quantization levels, where n is in a range of about two to about eight (col. 3 lines22 – 25) and the output is read out at 2n times the clock rate of the sigma-delta modulator (col. 4 lines 36 – 38) (i.e. wherein said over sampling modulator generates an over sampled signal having a period and a total number of levels, and wherein said clock rate is at least M times said period, where M is said total number of levels in said over sampled signal).

9. Regarding Claim 11, in addition to the elements stated above regarding claim 1, Ruha discloses a feedback path through the error measurement block (which includes the digital filter) (fig. 4) (i.e. a feedback path comprising said digital filter).

10. Regarding Claims 12 and 31, in addition to the elements stated above regarding claims 1 and 24, Ruha further discloses the signal processing system is integrated in

digital CMOS (fig. 40 (i.e. an integrated circuit chip system comprising the signal processor of claim 1).

11. Regarding Claims 21 and 34, in addition to the elements stated above regarding claims 1 and 24, Ruha discloses a switching stage that is used to drive an external load (col. 4 lines 19 – 20) (i.e. an audio power amplification system).

12. Regarding Claim 42, in addition to the elements stated above regarding claim 24, Ruha discloses the sample rates are the same (col. 4 lines 32 – 46) (i.e. wherein said sampling occurs at a clock rate of said pulse width modulator).

13. Regarding claim 47, Ruha discloses a sigma delta modulator that interpolates an input signal to an over sampled lower resolution (col. 4 lines 23 – 25), a pulse width modulator (fig. 4 element 12) and a feedback path through the error measurement block (which includes the digital filter) (fig. 4) (i.e. a digital over sampling circuit coupled with a digital pulse width modulating circuit having an output; and a feedback path comprising a digital filter that samples said output in a digital domain).

14. Regarding Claim 48, Ruha discloses inputting an N-bit signal, operating on it, a pulse width modulator (Fig. 4), a clock which affects the resolution of the PWM (col. 6 lines 49 – 50), the circuitry operates to minimize noise in the signal applied to the load . (col. 6 lines 62 – 63), and Ruha further discloses the signal processing system is integrated in digital CMOS (fig. 40) (i.e. an integrated circuit chip configured to receive a pulse code modulated digital signal and to generate a pulse width modulated digital output signal wherein said output signal has a distortion, and wherein said distortion is

suppressed by a digital filter that operates at least a clock rate of said pulse width modulated digital signal).

15. Regarding Claims 49 and 68, Ruha discloses a sigma delta modulator that interpolates the high accuracy input signal (e.g. 13 – 16 bits) to an over sampled lower resolution but multi-bit (e.g. 2 bit to 8 bit) (i.e. modulating a first pulse code modulated signal having a first resolution into a second pulse code modulated signal having a second resolution, wherein said second resolution is smaller than said first resolution), this signal is then applied to a pulse width modulator (fig. 4 elements 12 and 14) which has a clock rate (col. 6 lines 49 – 50) (i.e. modulating said second pulse code modulated signal into a third signal comprising a plurality of pulses in time having a clock rate), and an error measurement block that includes a digital filter (fig. 4 elements 16 and fig. 6B element 16c) which receives an input from the pulse width modulator (fig 4 element 14) and the circuitry operates to minimize noise in the signal applied to the load (col. 6 lines 62 – 63) (i.e. filtering in a digital domain said plurality of pulses in time to suppress a distortion in said third signal).

16. Regarding Claims 50 and 51 and 73, in addition to the elements stated above regarding claim 49, Ruha discloses a sigma delta modulator that interpolates the high accuracy input signal (e.g. 13 – 16 bits) (this range includes 16 bits) (i.e. wherein said first resolution is between 12 bits and 24 bits inclusively and wherein said first resolution is 16 bits).

17. Regarding Claims 52 and 53, in addition to the elements stated above regarding claim 50, Ruha discloses an over sampled lower resolution but multi-bit (e.g. 2 bit to 8

bit) (this range includes 4 bits) (i.e. wherein said second resolution is between 2 bits and 6 bits inclusively and wherein said second resolution is 4 bits).

18. Regarding Claim 54 in addition to the elements stated above regarding claim 49, Ruha discloses a sigma delta modulator that interpolates the high accuracy input signal (e.g. 13 – 16 bits) (i.e. wherein said modulating said first pulse code modulated signal comprises using a sigma-delta type modulator).

19. Regarding claim 56, in addition to the elements stated above regarding claim 49 Ruha discloses the signal from the sigma delta modulator is applied to a pulse width modulator (fig. 4 elements 12 and 14) (i.e. wherein said modulating said second pulse code modulated signal comprises using a pulse width modulator).

20. Regarding Claim 57 in addition to the elements stated above regarding claim 49, Ruha discloses an error measurement block that includes a digital filter (fig. 4 elements 16 and fig. 6B element 16c) which receives an input from the pulse width modulator (fig 4 element 14) (i.e. wherein said filtering comprises using a digital filter).

21. Regarding Claim 61, discloses a feedback signal filtered and then input to the sigma delta modulator (fig. 4) that interpolates the high accuracy input signal (e.g. 13 – 16 bits) (i.e. wherein said filtering comprises forming a feedback signal having said first resolution).

22. Regarding Claim 62, in addition to the elements stated above regarding claim 49, Ruha discloses a pulse width modulator (fig. 4 element 12) a clock which affects the resolution of the PWM (col. 6 lines 49 – 50) (i.e. a pulse width modulator having a clock rate) and an error measurement block that includes a digital filter (fig. 4 elements 16

and fig. 6B element 16c) which receives an input from the pulse width modulator (fig 4 element 14) (i.e. wherein said plurality of pulses in time is a substantially small range of pulses in time).

23. Regarding claim 63, in addition to the elements stated above regarding claim 63, Ruha discloses the output from the sigma-delta modulator has $2^n$ quantization levels, where n is in a range of about two to about eight (col. 3 lines22 – 25) and the output is read out at 2n times the clock rate of the sigma-delta modulator (col. 4 lines 36 – 38) (i.e. wherein said modulating said first pulse code modulated signal comprises generating an over sampled signal having a period and a total number of levels, wherein said modulating said second pulse code modulated digital signal occurs at a clock rate that is at least M times said period, where M is said total number of levels in said over sampled signal).

24. Regarding Claim 64, in addition to the elements stated above regarding claim 49, Ruha discloses a pulse width modulator (fig. 4 element 12) a clock which affects the resolution of the PWM (col. 6 lines 49 – 50) (i.e. a pulse width modulator having a clock rate) and an error measurement block that includes a digital filter (fig. 4 elements 16 and fig. 6B element 16c) which receives an input from the pulse width modulator (fig 4 element 14) (i.e. wherein said filtering comprises sampling at said clock rate).

***Claim Rejections - 35 USC § 103***

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 22 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruha (US Patent 6,466,087).

27. Regarding Claims 22 and 35, in addition to the elements stated above regarding claims 21 and 34, Ruha discloses a switching stage that is used to drive an external load and typically the block will contain an LC filter (col. 4 lines 19 – 20). An LC is one of many various L-R-C network filter configurations that could be used to accomplish the necessary filtration. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an RC filter in place of the LC filter discloses by Ruha to achieve similar results.

28. Claims 6, 27 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruha (US Patent 6,466,087) in view of Huang (U.S. Patent Application Pub 2004/0213333).

29. Regarding Claims 6, 27 and 55, in addition to the elements stated above regarding claims 5, 26 and 54, Huang discloses a First Order sigma delta modulator (Fig. 2) (i.e. wherein said sigma delta type modulator comprises a first order sigma-delta type modulator). It would have been obvious to one of ordinary skill in the art to use Huang's sigma delta modulator as Ruha's sigma delta modulator. It is considered

merely as one of several straightforward possibilities from which the skilled person would select in accordance with circumstances, without the exercise of inventive skill.

30. Claims 7, 30, 43, 44, 69 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruha (US Patent 6,466,087) in view of Groves Jr. (U.S. Patent 6,593,807).

31. Regarding Claims 7 and 30, in addition to the elements stated above regarding claims 3 and 25, Groves Jr. discloses a noise-shaping filter upstream of a pulse width modulation block (fig.2 and col. 1) (i.e. a filter upstream of said pulse width modulator). One of ordinary skill in the art at the time of the invention would have been motivated to add Groves Jr.'s noise shaping filter to improve the audio quality of the signal (Groves Jr. Col. 1).

32. Regarding Claim 43, Ruha discloses a sigma delta modulator that interpolates an input signal to an over sampled lower resolution (col. 4 lines 23 – 25), a pulse width modulator (fig. 4 element 12) (i.e. a forward path with an encoder stage, wherein said encoder stage comprises a first order sigma-delta type modulator and a pulse width modulator), the output from the sigma-delta modulator has $2^n$ quantization levels, where n is in a range of about two to about eight (col. 3 lines22 – 25) and the output is read out at 2n times the clock rate of the sigma-delta modulator (col. 4 lines 36 – 38) (i.e. wherein said sigma-delta type modulator generates an over sampled signal having a period and a total number of levels, and said pulse width modulator operates at a clock rate that is at least M times said period, where M is said total number of levels in said over sampled signal and where forward path produces an output having a distortion)

and a feedback path through the error measurement block (which includes the digital filter) (fig. 4) (i.e. a feedback path comprising a digital filter that samples said output in a digital domain to suppress said distortion. Ruha does not disclose a first filter stage couple with and upstream from an encoder. Groves Jr. discloses a noise-shaping filter upstream of a pulse width modulation block (fig.2 and col. 1) (i.e. a first filter stage couple with and upstream from an encoder). One of ordinary skill in the art at the time of the invention would have been motivated to add Groves Jr.'s noise shaping filter to improve the audio quality of the signal (Groves Jr. Col. 1).

33. Regarding claim 44, in addition to the elements stated above regarding claim 43, Ruha discloses the output is read out at 2n times the clock rate of the sigma-delta modulator (col. 4 lines 36 – 38) (i.e. wherein said digital filter samples said output at said clock rate).

34. Regarding Claims 69 and 70, in addition to the elements stated above regarding claims 7 and 30, Ruha discloses a switching stage that is used to drive an external load and typically the block will contain an LC filter (col. 4 lines 19 – 20). An LC is one of many various L-R-C network filter configurations that could be used to accomplish the necessary filtration. An RC integrator is also one of many choices that could be implemented. It would have been obvious to one of ordinary skill in the art at the time of the invention to use an RC integrator filter in place of the LC filter discloses by Ruha to achieve similar results. It would be desirable to use an integrator in order to achieve a linear frequency response. A linear frequency response is necessary in audio applications in order to maintain signal quality.

35. Claims 8 – 10 and 58 - 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruha (US Patent 6,466,087) in view of Lis (U.S. Patent Application Pub 2004/0037432).

36. Regarding Claims 8 and 58, in addition to the elements stated above regarding claims 1 and 49, Lis discloses a low-pass filter (e.g., IIR filter) having a single pole (paragraph 31) (i.e. wherein said digital filter comprises an IIR filter). It would have been obvious to one of ordinary skill in the art to use Lis' single pole LP digital filter as Ruha's digital filter. It is considered merely as one of several straightforward digital filter possibilities from which the skilled person would select in accordance with circumstances, without the exercise of inventive skill.

37. Regarding Claims 9 and 59, in addition to the elements stated above regarding claims 8 and 58, Lis discloses a low-pass filter (e.g., IIR filter) having a single pole (paragraph 31) (i.e. wherein said IIR filter comprises a single pole filter).

38. Regarding Claims 10 and 60, in addition to the elements stated above regarding claims 1 and 57, Lis discloses a low-pass filter (e.g., IIR filter) having a single pole (paragraph 31) (i.e. wherein said digital filter comprises a low pass filter).

39. Claims 13, 14, 31, 32 and 65 - 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruha (US Patent 6,466,087) in view of Bedini (U.S. Patent 4,555,795).

40. Regarding Claims 13, 14, 32, and 33, in addition to the elements stated above regarding claims 12 and 31, Ruha discloses a load block that typically contains a speaker (monaural output) (fig. 4 element 15 and col. 4 lines 19 – 22). Bedini discloses

a binaural audio processor that can be cascaded together to provide multiple channels from a monaural input and as few as two and as many as eight channels could be provided (col. 9 lines 21 – 38) (i.e. a two-channel output or an eight-channel output). One of ordinary skill in the art at the time of the invention would have been motivated to use Bedini's processor in conjunction with Ruha's invention in order to provide a more pleasing sound for the listener. Bedini discloses that the processor would allow a monaural input to provide strategic placing of speakers around a theater to surround the audience with sound (col. 9 lines 29 – 32).

41. Regarding claim 65, in addition to the elements stated above regarding claim 49, Bedini further discloses a left and right bass boost channel (fig. 2 elements 32 and 34) Using this in the same manner as above regarding claims 13, 14, 31 and 32 will provide an amplified output (i.e. further comprising amplifying said third signal to produce an amplified output). Motivation to combine these elements is listed above regarding claims 13, 14, 31 and 32.

42. Regarding Claim 66, in addition to the elements stated above regarding claim 65, Bedini discloses a processor that works on analog signals (i.e. creating an analog signal from said amplified output).

43. Regarding Claim 67, in addition to the elements stated above regarding claim, Ruha discloses a switching stage that is used to drive an external load and typically the block will contain an LC filter (col. 4 lines 19 – 20). An LC is one of many various L-R-C network filter configurations that could be used to accomplish the necessary filtration. It

would have been obvious to one of ordinary skill in the art at the time of the invention to use an RC filter in place of the LC filter discloses by Ruha to achieve similar results.

44. Claims 15 - 20 and 36 – 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruha (US Patent 6,466,087) in view of Terui (U.S. Patent 5,903,871).

45. Regarding Claims 15 and 36, in addition to the elements stated above regarding claims 1 and 24, Terui discloses a portable audio player (entire document) (i.e. a portable audio player). One of ordinary skill in the art at the time of the invention would have been motivated to use Ruha's invention on Terui's portable player to efficiently playback audio with minimal error and distortion.

46. Regarding Claims 16 and 37, in addition to the elements stated above regarding claims 15 and 36, Terui further discloses a recording medium for storing digital audio data (col. 4 lines 50 - 59) (i.e. a digital audio signal source).

47. Regarding Claims 17, 18, 38, and 39, in addition to the elements stated above regarding claims 15 and 36, Terui further discloses the main recording medium portion uses a magneto-optical disc (col. 5 lines 3 – 4) (i.e. an optical disk reader).

48. Regarding Claims 19 and 40, in addition to the elements stated above regarding claims 16 and 37, Terui further discloses a recording medium for storing digital audio data (col. 4 lines 50 – 59) (i.e. a memory for storage of a digital audio file).

49. Regarding Claims 20 and 41, in addition to the elements stated above regarding claims 16 and 37, Terui further discloses that the recording medium receives digital audio from the main control circuit (col. 4 lines 50 – 59) (i.e. wherein said digital audio signal source comprises a digital receiver).

50. Claims 45 and 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruha (US Patent 6,466,087) in view of Groves Jr. (U.S. Patent 6,593,807) and in further view of Izandpanah (U.S. Patent 6,735,398).

51. Regarding claim 45, in addition to all of the elements stated above regarding claim 43, Izandpanah discloses a pulse width transmission scheme which allows for a channel modulation depth of +/- 22.5% (col. 7 lines 11 – 22). 1 db is equal to a magnitude change of approximately 20% (i.e. wherein said signal processor exhibits a modulation depth of up to about – 1db in an audio frequency band). One of ordinary skill in the art at the time of the invention would have been motivated to use Izandpanah's modulation scheme on the Ruha and Groves Jr. combination in order to ensure quality transmission of signals.

52. Regarding claim 71, in addition to all of the elements stated above regarding claim 43, Izandpanah discloses a pulse width transmission scheme which allows for a channel modulation depth of +/- 22.5%. 0 db is equal to a magnitude change of approximately 0% (i.e. wherein said signal processor exhibits a modulation depth of up to about 0 db in an audio frequency band). One of ordinary skill in the art at the time of the invention would have been motivated to use Izandpanah's modulation scheme on the Ruha and Groves Jr. combination in order to ensure quality transmission of signals.

53. Claims 46 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ruha (US Patent 6,466,087) in view of Groves Jr. (U.S. Patent 6,593,807) and in further view of Pennock (U.S. Patent 6,573,850).

54. Regarding Claim 46 and 72, in addition to the elements stated above regarding claim 43, Pennock discloses a delta sigma converter with a total Harmonic distortion of –100 db (col. 1 lines 12 – 25) (i.e. wherein signal processor reduces a total harmonic distortion to about 90 – 100 db and wherein said signal processor reduces a total harmonic distortion to about 90 – 140 db). One of ordinary skill in the art at the time of the invention would have been motivated to use Pennock's noise level on the Ruha and Groves Jr. combination in order to ensure quality signal transmission.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C Flanders whose telephone number is (703) 305-0381. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forrester Isen can be reached on (703) 305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

acf

HUYEN LE
PRIMARY EXAMINER